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| 10/795,981 | 03/10/2004 | Hisashi Nagata | 1035-499 | 2189 |

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| EXAMINER | |
|---|---|
| DUONG, THOI V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2871 | |

DATE MAILED: 10/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/795,981 | NAGATA ET AL. | |
| | Examiner | Art Unit | |
| | Thoi V. Duong | 2871 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *9-15,28,35-37 and 42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-15,28,35-37 and 42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/520,609.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to the Amendment filed August 28, 2006.

Accordingly, claims 14 and 42 were amended, and claims 1-8, 16-27, 29-34 and 38-41 were cancelled. Currently, claims 9-15, 28, 35-37 and 42 are pending in this application.

### *Allowable Subject Matter*

2. The indicated allowability of claims 9-13, 28 and 35-37 are withdrawn in view of the newly discovered reference, US 6,456,350 B1 to Ashizawa et al.. Rejections based on the newly cited reference(s) follow.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 9, 10, 12, 13 and 42 are rejected under 35 U.S.C. 102(e) as being anticipated by Ashizawa et al. (Ashizawa, US 6,456,350 B1).

Re claim 9, as shown in Figs. 2 and 3, Ashizawa discloses an active matrix substrate SUB1, comprising:

a pixel electrode PX provided in a pixel area;

a scanning line GL and a signal line DL;

a switching element TFT electrically connected to the scanning line GL, the signal line DL, and the pixel electrode PX;

a storage capacitor electrode CL for a storage capacitor Cstg (col. 6, lines 44-48); and

a storage capacitor common line CC3 disposed parallel to the signal line DL so as to be electrically connected to the storage capacitor electrode CL, the storage capacitor common line extending across a plurality of pixels PX (Figs. 2 and 3C), wherein storage capacitance is provided between the pixel electrode PX and the storage capacitor electrode CL (col. 6, lines 44-48),

the scanning line GL and the storage capacitor electrode CL are fabricated from a same material in a single patterning (col. 5, lines 30-33); and

wherein the storage capacitor electrode CL and the storage capacitor common line CC3 are patterned in different steps so as to have an insulating film PAS1 provided partially therebetween (Fig. 3C and col. 6, lines 23-26).

Re claim 10, as shown in Figs. 3A-3C, the signal line DL and the pixel electrode PX are fabricated from a single conductive layer through patterning thereof.

Re claim 13, the active matrix substrate further comprises a gate insulation film PAS1 for covering a gate electrode GT of the switching element TFT, wherein the pixel electrode PX is disposed opposing the storage capacitor electrode CL across the gate insulation film.

Re claim 12, as shown in Figs. 2 and 3, Ashizawa discloses an active matrix substrate SUB1, comprising:

a pixel electrode PX provided in a pixel area;

a scanning line GL and a signal line DL;

a switching element TFT electrically connected to the scanning line GL, the signal line DL, and the pixel electrode PX;

a storage capacitor electrode CL for a storage capacitor Cstg (col. 6, lines 44-48); and

a storage capacitor common line CC3 disposed at least partially parallel to the signal line DL so as to be electrically connected to the storage capacitor electrode CL, the storage capacitor common line CC3 extending across a plurality of pixels (Figs. 2 and 3C), wherein

storage capacitance is provided between the pixel electrode PX and the storage capacitor electrode CL (col. 6, lines 44-48),

the scanning line GL and the storage capacitor electrode CL are fabricated from a same material in a single patterning (col. 5, lines 30-33); and

wherein in another patterning the signal line DL, the pixel electrode PX, and the storage capacitor common line CC3 are fabricated of a same material in a single patterning (Figs. 3A-3C).

Re claim 42, as shown in Figs. 2 and 3, Ashizawa discloses an active matrix substrate comprising:

a pixel electrode PX provided in each pixel area bounded by a scanning line GL and a signal line DL that are disposed in a matrix as a whole;

a switching element TFt connected to the scanning line GL, the signal line DL, and the pixel electrode PX;

a storage capacitor electrode CL for constituting a storage capacitor Cstg (col. 6, lines 44-48); and

a storage capacitor common line CC3 disposed parallel to the signal line DL so as to be connected to the storage capacitor electrode CL, the storage capacitor common line CC3 extending across a plurality of pixels (Figs. 2 and 3C), wherein

the storage capacitor Cstg is formed between the pixel electrode PX and the storage capacitor electrode CL (col. 6, lines 44-48),

the scanning line GL and the storage capacitor electrode CL are fabricated from a single electrode layer through patterning thereof (col. 5, lines 30-33), and

the signal line DL and the storage capacitor common line CC3 are fabricated of a same material in a single patterning thereof (Figs. 3A-3C and col. 6, lines 23-26).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 11, 14,15 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ashizawa et al. (Ashizawa, US 6,456,350 B1) in view of Oh et al. (Oh, US 6,211,928 B1).

Re claim 14, as shown in Figs. 2 and 3, Ashizawa discloses an active matrix substrate SUB1, comprising:

a pixel electrode PX provided in a pixel area;

a scanning line GL and a signal line DL;

a switching element TFT electrically connected to the scanning line GL, the signal line DL, and the pixel electrode PX;

a storage capacitor electrode CL for a storage capacitor Cstg (col. 6, lines 44-48); and

a storage capacitor common line CC3 disposed at least partially parallel to the signal line DL so as to be electrically connected to the storage capacitor electrode CL, the storage capacitor common line CC3 extending across a plurality of pixels (Figs. 2 and 3C), and wherein the signal line DL and the storage capacitor common line CC3 are fabricated of a same material in a single patterning (col. 6, lines 23-26), wherein

storage capacitance Cstg is provided between the pixel electrode PX and the storage capacitor electrode CL (col. 6, lines 44-48),

the scanning line GL and the storage capacitor electrode CL are fabricated from a same material in a single patterning (col. 5, lines 30-33); and

a protection film PAS2 for covering the switching element TFT.

Kakuda discloses an active matrix substrate that is basically the same as that recited in claims 11 and 14 except for an interlayer insulation film interposed between the pixel electrode and the protection film.

As shown in Fig. 8J, Oh discloses an active matrix substrate comprising a protection film 126 (passivation film), a pixel electrode 104, and an insulation film 156 (planarization film) interposed between the pixel electrode 104 and the protection film 126 (col. 5, lines 28-63).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the active matrix substrate of Ashizawa with the teaching of Oh by forming an interlayer insulating film interposed between the pixel electrode and the protection film in order to obtain a smooth surface profile to alleviate the steps of multi-layer structure underneath, provide a uniform cell gap and improve the display quality by reducing instability in filling liquid crystal in the gap (col. 5, lines 48-52).

Re claim 15, as shown in Figs. 8J and 9A, Oh discloses a contact hole formed through the interlayer insulation film 156 and the protection film 126 in order to

electrically connect the pixel electrode 104 to the switching element TFT 108 (col. 5, lines 56-60).

Re claim 28, as shown in Fig. 8B, Oh discloses that the gate electrode 117a is anodized to form an anodized film 135 to prevent hillocks and improve electrical insulation (col. 5, lines 9-12). Accordingly, it is obvious that the scanning line is anodized to prevent hillocks and improve electrical insulation.

7. Claims 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ashizawa et al. (Ashizawa, US 6,456,350 B1) in view of Jeromin et al. (8.4: Application of a-Si Active-Matrix Technology in a X-Ray Detector Panel).

Re claim 35, as shown in Figs. 2 and 3, Ashizawa discloses an active matrix substrate, comprising:

a pixel electrode PX provided in a pixel area;

a scanning line GL and a signal line DL;

a switching element TFT electrically connected to the scanning line GL, the signal line DL, and the pixel electrode PX

a storage capacitor electrode CL for a storage capacitor Cstg (col. 6, lines 44-48); and

a storage capacitor common wire CC3 disposed at least partially parallel to the signal line DL so as to be electrically connected to the storage capacitor electrode CL (Figs. 2 and 3C), wherein the scanning line GL and the storage capacitor electrode CL are fabricated from a same material in a single patterning (col. 5, lines 30-33); and

wherein the storage capacitor electrode CL and the storage capacitor common wire CC3 are patterned in different steps so as to have an insulating film PAS1 provided partially therebetween (Fig. 3C).

Re claim 36, Ashizawa further discloses a gate insulation film PAS1 for covering a gate electrode GT of the switching element TFT; and a conductive body layer (horizontal portion of the pixel electrode PX) deposited on the gate insulation film PAS1 so as to be connected to the switching element TFT, wherein

the storage capacitor electrode CL and the conductive body layer constitute the storage capacitor Cstg across the gate insulation film PAS1 (col. 6, lines 44-48).

Ashizawa discloses an active matrix substrate that is basically the same as that recited in claim 34 except for an image sensor comprising a conversion section for converting incident magnetoelectric radiation to electric charges and bias voltage application means for causing a storage capacitor to store the electric charges.

In "Application of a-Si Active-Matrix Technology in a X-Ray Detector Panel" cited by Applicant, Jeromin discloses an active matrix substrate used in X-ray detector panel comprising amorphous selenium which converts x-ray photons into charge carrier pairs. Jeromin also discloses that the positive charges are collected in the storage capacitors of the pixels and are then read out charge amplifiers connected to the source lines (see Abstract). Accordingly, a conversion section for converting incident magnetoelectric radiation to electric charges and bias voltage application means for causing a storage capacitor to store the electric charges are to be employed in the X-Ray detector panel.

Thus, as intended purpose, it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the active matrix substrate of Ashizawa in the image sensor of Jeromin comprising a conversion section for converting incident magnetoelectric radiation to electric charges and bias voltage application means for causing a storage capacitor to store the electric charges for obtaining the actual x-ray image (page 93, col. 2).

8. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ashizawa et al. (Ashizawa, US 6,456,350 B1) in view of Jeromin et al. (8.4: Application of a-Si Active-Matrix Technology in a X-Ray Detector Panel) as applied to claims 35 and 36 above and further in view of Oh et al. (Oh, USPN 6,211,928 B1).

Ashizawa as modified in view of Jeromin above includes all that is recited in claim 38 except for the scanning line being anodized.

As shown in Fig. 8J, Oh discloses that the scanning line 117a is anodized to form an anodized film 135 to prevent hillocks and improve electrical insulation (col. 5, lines 9-12).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the active matrix substrate of Ashizawa with the teaching of Oh by anodizing the scanning line to prevent hillocks and improve electrical insulation (col. 5, lines 9-12).

***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-

2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached at (571) 272-1787.

Thoi V. Duong

10/20/2006